

# Live Demonstration: An Associative Capacitive Network Based on Nanoscale Complementary Resistive Switches

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**Abstract**—Integration density is a major drawback of today's associative memories required for intelligent data processing for such as pattern recognition or classification. Ultra dense complementary resistive switch-based architectures are thought to overcome this issue, offering a footprint of  $4F^2$ . Here we demonstrate the feasibility of an 8 by 16 associative capacitive network.

**Keywords**—associative network, complementary resistive switch, memristive device, resistive memory

## I. INTRODUCTION

Complementary resistive switches (CRS) are emerging two terminal memristive devices offering inherent sneak path prevention and low power consumption [1]. CRS devices are suited for ultra-dense  $4F^2$  non-volatile memory applications. By engineering different capacitance values to each part cells, a non-destructive capacitive read-out is feasible [2], which can be exploited for implementation of associative capacitive networks (ACN) [3]. ACNs are capable of performing fully parallel recognition tasks, evaluating the Hamming distances between stored and input patterns (Fig. 1).

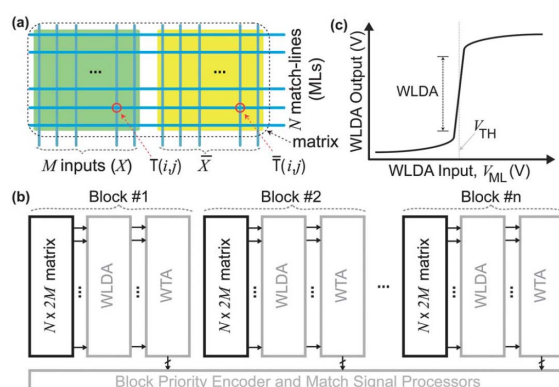


Fig. 1. ACN architecture. Taken from [3].

In [3] we have introduced the basic concept which we want to demonstrate live. The topic matches the ISCAS track selection 'Neural Systems and Applications' and the CAS-FEST topic on 'Memristive devices, circuits, systems and applications'.

## II. DEMONSTRATION SETUP AND VISITOR EXPERIENCE

Fig. 2a shows the ACN chip which is bonded to a 28-pin chip carrier. An 8 by 16 associative array is depicted (Fig. 2b).

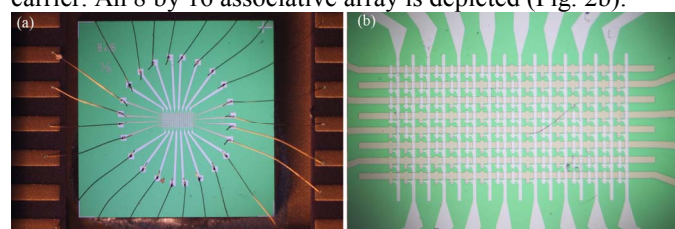


Fig. 2. (a) Experimental ACN network (8 by 16) array with  $4 \times 10 \mu m^2$  and  $20 \times 10 \mu m^2$  cells bonded to a 28-pin chip carrier. (b) High resolution image of the ACN array.

The basic measurement unit (MU) is depicted in Fig. 13. A pulse generator gives the input signal to the MU, generating the search pattern and addressing the ACN chip. The ACN match line signals are evaluated by the MU which can be displayed by an oscilloscope. Further details for of the required hardware blocks can be found in [3].

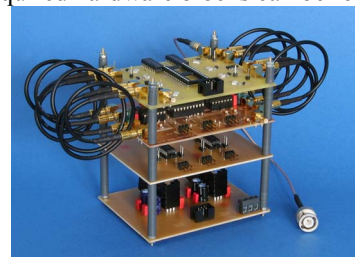


Fig. 3. External circuitry receiving input signals and evaluating the Hamming distances. The chip carrier providing the CAN array is inserted on top. Additional hardware: pulse generator and oscilloscope.

## REFERENCES

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